REMARKS

The application has been carefully reviewed in light of the Office Action dated May 21, 2003. Claims 1, 16, 17, 19 and 20 have been amended. Claims 1-20 are pending in this case.

The specification stands objected to due to certain informalities. Reconsideration is respectfully requested. The specification has been amended in response to the objection. The application as amended is believed to be in proper form.

Claims 1-4, 6, 8-14 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakajima et al. (U.S. Patent No. 6,181,314 B1) in view of Negishi et al. (U.S. Patent No. 5,528,241) and further in view of Yamagata et al. (U.S. Patent Application Publication No. US# 2001/0028336 A1). Applicants respectfully traverse the rejection and request reconsideration.

In Fig. 2 of Nakajima, n output buffers 16 are connected between output circuit 17 and capacitance loads C1 to Cn through analog switches 18-1 to 18-n, which creates a problem since building in as many analog circuits as signal lines pulls down the yield of the display unit. (see specification page 1, lines 11-13). Claim 1 includes a drive unit comprising a ladder resistor, impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters, and a gray level voltage selector connected to the gray level voltage wires.

An outstanding effect of the present invention is the fact that analog active circuits, such as impedance converters, need not be as many as the number of signal lines, but are sufficient in the same number as the gray level voltage wires. Calculation of this factor by a panel of common intermediate format (CIF) of four-bit display data, whose common pixel electrodes are A.C. driven, reveals a reduction from (352 x RGB = 1056) to 24 – 16, which represents a significant yield enhancement. (see specification page 3, lines 15-23). Another aspect of the present invention is the use of first, second and third phases for writing an analog image signal voltages using impedance converters.

Nakajima fails to disclose (or render obvious) all of the limitations of claim 1. For example, Nakajima does not disclose impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters, and a gray level voltage selector connected to the gray level voltage wires. To the contrary, Nakajima as shown in FIG. 2 merely discloses the transfer of a data signal from D/A converters 15 through impedance converters 17 to signal lines 20.

The device of claim 1 differs from Nakajima since the number of impedance converters need not be as many as the number of signal lines as in Nakajima. Nakajima also fails to teach or suggest or suggest the structure of claim 1 and the order of signal transferring phases of the present invention.

Further, please note that neither Negishi nor Yamagata discloses impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters, and a gray level voltage selector connected to the gray level voltage wires. The digital to analog converter disclosed in Negishi is merely a converter that includes a ladder-resistor type which includes serially connected 256 resistors R1..R256 of the same resistance value. A switch portion selectively connects junction points of the resistors to an input terminal of an amplifier to a second reference voltage.

The integrated circuit disclosed in Yamagata includes an impedance converter, a ladder resistor, and gradation levels with six N-channel MOS transistors (transfer gates) Tr that are connected to respective negative gradation voltage lines NLN in series. The N-channel MOS transistors Tr are arranged as a two-dimensional matrix of 6 rows.times.64 columns. A signal line 3 from the negative data latch LT1 (FIG. 1) is connected to the gates of each transistor Tr. Depending upon a digital image data supplied to the signal line 3, one of sixty-four negative gradation voltage lines NLN is selected to output an analog gradation voltage to the negative operational amplifier OP1 (FIG. 1) via the signal line 4.

Thus, the proposed combination does not teach or suggest the invention as claimed. The combination of Nakajima, Negishi and Yamagata does not teach or suggest

all of the limitations of claim 1. Therefore, the rejection of claim 1 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 2-15 depend from claim 1 and are allowable over the combination of Nakajima, Negishi and Yamagata for the reasons mentioned above with respect to claim 1, and also because Nakajima fails to teach or suggest the respective inventive combinations defined by claims 2-15. Likewise, claims 16-20 should be allowed for at least for the reasons mentioned above with respect to claim 1.

Further, please note that Kane does not disclose a method wherein a plurality of gray level voltage wires connected to an output of the ladder resistor, a group of signal lines connected to the gray level voltage wires via a gray level voltage selector where each gray level voltage wire is connected to the output of the ladder resistor via impedance converters. Also, Kane does not teach or suggest a method wherein analog image signal voltages are written into an image display apparatus having a drive unit including a ladder resistor, impedance converters connected to an output of a ladder resistor. Neither does Kane teach or suggest gray level voltage wires constituting output lines connected to the impedance converters, and a gray level voltage selector connected to the gray level voltage wires in three separate phases when the analog image signal voltages are written onto the signal lines.

Kane merely discloses a method to improve brightness uniformity by reducing current nonuniformities in a light-emitting diode in a pixel structure. This is an additional reason why claims 16 and 19 should be allowable over the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: August 21, 2003

Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant

(202)887-0689